CLAIMS

WHAT IS CLAIMED:

1. A method of forming spacer elements, the method comprising:

forming a conductive line above a semiconductor region;

conformally forming a spacer layer stack over said conductive line and said semiconductor region, said spacer layer stack comprising an etch stop layer separating a first spacer layer from a second spacer layer formed above said first spacer layer, said first and second spacer layers comprised of a material that may be etched selectively to said etch stop layer by a predefined etch chemistry;

anisotropically etching said second spacer layer to form sacrificial sidewall spacers;

removing portions of said etch stop layer that are exposed during the formation of said sacrificial sidewall spacers; and

removing said sacrificial sidewall spacers and exposed portions of said first spacer layer by an etch process using said specified etch chemistry to form said spacer elements.

2. The method of claim 1, wherein said sacrificial sidewall spacers and exposed portions of said first spacer layer are removed by a common etch process.

3. The method of claim 1, further comprising forming a second etch stop layer under said spacer layer stack.

4. The method of claim 3, wherein said second etch stop layer is comprised of the same material as said etch stop layer.

5. The method of claim 4, further comprising removing exposed portions of said second etch stop layer.

6. The method of claim 1, wherein said sacrificial sidewall spacers and exposed portions of said first spacer layer are removed by an isotropic etch process.

7. The method of claim 1, wherein said first and second spacer layers are comprised of substantially the same material.

8. The method of claim 7, wherein said first and second spacer layers are comprised of silicon nitride.

9. The method of claim 8, wherein said first and second spacer layers are formed by plasma enhanced chemical vapor deposition.

10. The method of claim 8, wherein said etch stop layer is comprised of silicon dioxide.

11. The method of claim 10, wherein said second etch stop layer is comprised of silicon dioxide.

12. The method of claim 6, further comprising controlling a degree of recessing said first spacer layer with respect to a top surface of said conductive line by correspondingly adjusting at least one process parameter of the isotropic etch process.

13. The method of claim 12, wherein said at least one process parameter represents at least one of an etch chemistry and an etch time.

14. The method of claim 1, wherein anisotropically etching said second spacer layer to form sacrificial sidewall spacers, removing portions of said etch stop layer that are exposed during the formation of said sacrificial sidewall spacers, and removing said sacrificial sidewall spacers and exposed portions of said first spacer layer by a common etch process using said specified etch chemistry performed as an *in situ* process.

15. The method of claim 1, further comprising adjusting a length of said conformal spacer element by controlling a thickness of said second spacer layer.

16. The method of claim 1, further comprising adjusting a thickness of said conformal spacer element by controlling a thickness of said first spacer layer.

17. The method of claim 1, wherein said conductive line represents a gate electrode of a field effect transistor receiving a lateral drain and source dopant profile that is controllable by the thickness and the length of said conformal spacer element.

18. The method of claim 1, wherein said sacrificial sidewall spacers are removed, at least partially, by an anisotropic etch process.

19. The method of claim 18, further comprising selecting a thickness of said etch stop layer on the basis of a height of said line and an etch selectivity of said anisotropic etch process.

20. The method of claim 19, wherein said exposed portions of said etch stop layer are removed, at least partially, during said anisotropic etch process.

21. A method of forming spacer elements, the method comprising:

forming a conductive line above a semiconductor region;

forming a spacer layer stack comprising a first etch stop layer formed of a first material, a first spacer layer formed of a second material, a second etch stop layer formed of said first material and a second spacer layer formed of said second material;

forming a sacrificial spacer at least from said second spacer layer; and

forming spacer elements at least from said first spacer layer by removing said sacrificial spacer.

22. The method of claim 21, wherein said second material comprises silicon nitride.

23. The method of claim 21, wherein said first material comprises silicon dioxide.

24. The method of claim 22, wherein said second material is deposited by plasma enhanced chemical vapor deposition.

25. The method of claim 21, wherein said sacrificial spacers are removed, at least partially, by an anisotropic etch process.

26. The method of claim 25, wherein said sacrificial spacers are substantially completely removed by an anisotropic etch process.

27. The method of claim 21, wherein said sacrificial sidewall spacers and exposed portions of said first spacer layer are removed by a common etch process.

28. The method of claim 21, further comprising removing exposed portions of said first and second etch stop layers.

29. The method of claim 21, wherein said sacrificial sidewall spacers and exposed portions of said first spacer layer are removed by an isotropic etch process.

30. The method of claim 29, further comprising controlling a degree of recessing said first spacer layer with respect to a top surface of said conductive line by correspondingly adjusting at least one process parameter of said isotropic etch process.

31. The method of claim 30, wherein said at least one process parameter represents at least one of an etch chemistry and an etch time.

32. The method of claim 21, wherein forming sacrificial sidewall spacers and forming said conformal spacer elements by removing said sacrificial sidewall spacers is performed as an *in situ* etch process.

33. The method of claim 21, further comprising adjusting a length of said conformal spacer element by controlling a thickness of said second spacer layer.

34. The method of claim 29, further comprising adjusting a length of said conformal spacer element by controlling at least one process parameter of said isotropic etch process.

35. The method of claim 21, further comprising adjusting a thickness of said conformal spacer element by controlling a thickness of said first spacer layer.

36. The method of claim 21, wherein said conductive line represents a gate electrode of a field effect transistor receiving a lateral drain and source dopant profile that is controllable by a thickness and a length of said conformal spacer element.